CSE460: VLSI Design Handout (Fall 2025)

## **Communication platform:**

## CSE460 Fall 2025 Official Discord Server: <https://discord.gg/YAwdFCuXH4>

## **Course Outcomes and Contents:**

Course Outline:[CSE460 - Course Outline.docx](https://docs.google.com/document/d/1b1V4cX4yTuAVefyebx_Pq8EPZrDkVUvO/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

| **Course Outcomes** | | **Course Contents** | |
| --- | --- | --- | --- |
| CO1 | Before Midterm | * Review of Digital Logic Design, * Logic design with CMOS, * CMOS DC Response | |
| CO2 | | * Finite State Machine design with logic gates | |
| CO3 | | * Delay and Power considerations in CMOS logic circuits | |
| CO4 | | * Algorithms in Physical Design - Partitioning Algorithm and Routing Algorithm | |

**CO Description and Weightage**

| **Sl.** | **CO Description** | **Weightage (%)** |
| --- | --- | --- |
| **CO1** | **Design** combinational and sequential circuits in CMOS by demonstrating the current voltage relationship and the dc response, and compute the noise margin of CMOS circuits. | 30% |
| **CO2** | **Construct** system design process using finite state machines and hardware description language. | 25% |
| **CO3** | **Analyze** the power dissipation and propagation delay of CMOS circuits. | 25% |
| **CO4** | **Devise** algorithms to design and optimize the physical layout of an IC. | 20% |

## **Marks distribution:**

| **Theory/Lab** | **Assessment** | **Percentage** | **Total number of assessments** | **Number of assessments to be graded** |
| --- | --- | --- | --- | --- |
| Theory  (75%) | Attendance | **-** | - | 70% (90%+ for lab) or more to be eligible for Final Exam |
| Assignment | **5%** | Count at least 2 | Variable section-wise |
| Quiz**\*** | **20%** | Count at least 3 | Best (n-1) |
| Midterm | **25%** | 1 | 1 |
| Final | **25%** | 1 | 1 |
| Lab  (25%) | Lab Performance | **12%** | 5 (n) | Best (n-2) |
| Lab-test | **6%+7%** | 2 | 2 |

**\***The last quiz (nth quiz) will be considered as a make-up for any missed quiz (maximum of 1), whatever the reason. **No other make-up quizzes will be taken.**

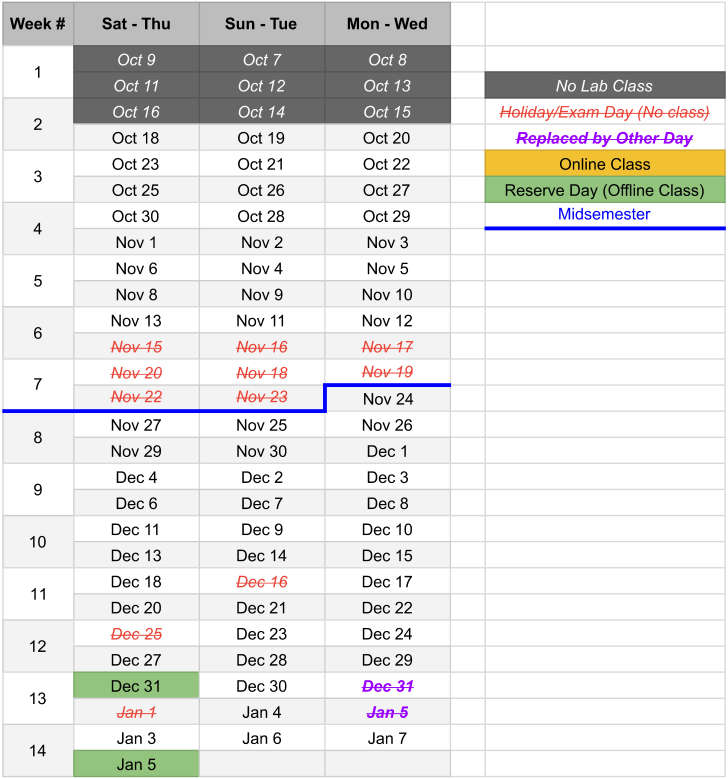
**Routine & Course Team:**

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## Course Team

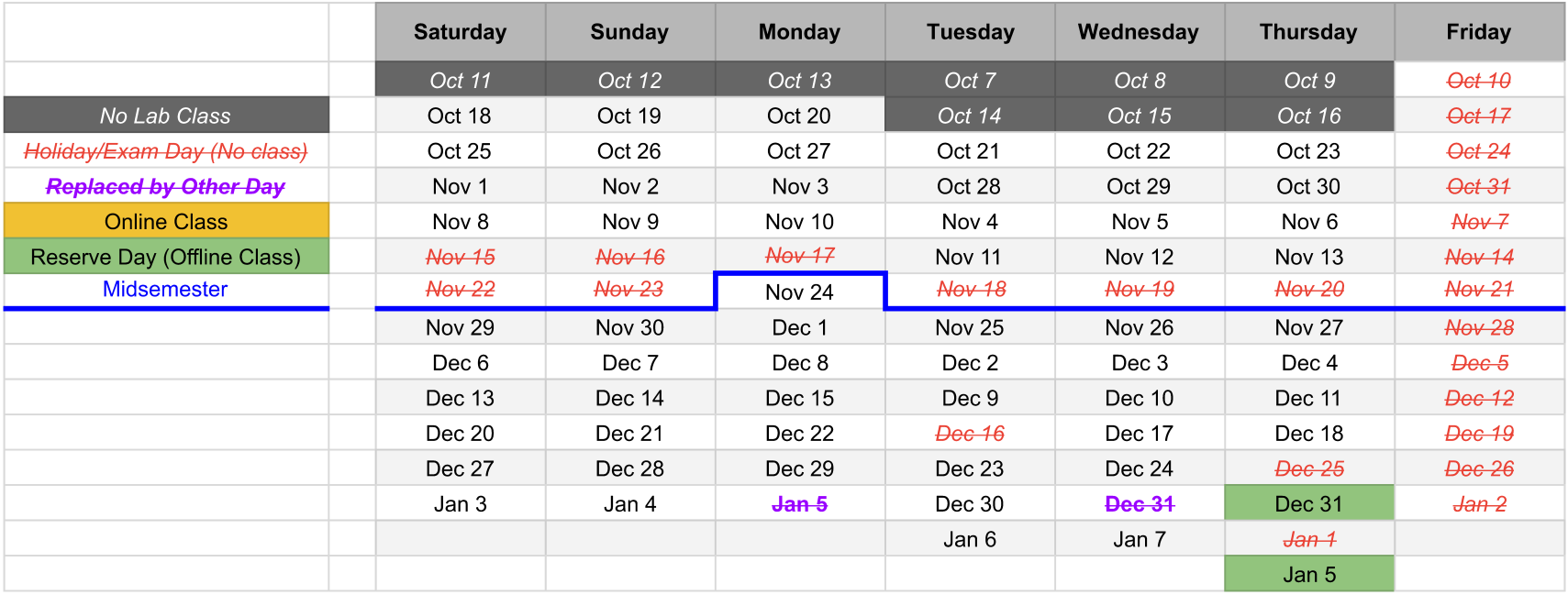
| **Initial** | **Name** | **BRACU Email** |
| --- | --- | --- |
| ARPD | Arpa Roy Dastider | ext.arpa.roy@bracu.ac.bd |
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| ZIZE | Zahin Iqbal Zeal | ext.zahin.ikbal@bracu.ac.bd |
| AASA | Abrar Al Shadid Abir | ext.abrar.abir@bracu.ac.bd |
| SDL | Shadmin Sultana | ext.shadmin.sultana@bracu.ac.bd |

**Schedule ( Theory ):**

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**Lab Schedule and Policy**

( need to update )



Lab policies:

1. No make-up of lab will be considered without valid reason. You need to submit valid medical documents in order to sit with any other section and obtain the permission from that section’s lab faculties, keeping your original lab faculties in the cc of the mail.
2. Make-up labs must be done by attending lab class with other sections. No make-up lab assessment shall be held during the consultation period.
3. If a student arrives more than 20 minutes after the lab has started, he/she will be marked as late. Late attendees will face a 30% deduction in their assessment marks for that particular day. If they arrive more than one hour after the lab has begun, they will be considered absent and must make up the class with another section.

# **Course contents**

Detailed List of Topics

Introduction to VLSI (Very Large Scale Integration) design: history, IC trends, technology & design approaches. Moore’s law. Review of digital logic design.

Introduction to logic circuit families: n-MOS, p-MOS, pseudo n-MOS and CMOS technologies. Introduction to CMOS logic. Pull-up and pull-down networks, implementation using series and parallel MOSFETs. Combinational logic circuit design using CMOS. Complex gate design using CMOS such as And-Or-Invert or Or-And-Invert. Implementation of different circuit elements like basic gates. Multiplexers, encoder, latch, flip-flops using CMOS.

Introduction to FSM (Finite State Machine): Moore type & Mealy type FSM hardware implementation. State encoding & minimization techniques.

DC Response of CMOS gates: n-MOS & p-MOS pass transistors. Logic levels and noise margins. DC transfer characteristics.

CMOS Power: instantaneous and average power, energy. Power analysis of circuit elements (R, C, DC Supply). Switching waveforms of an inverter. Static power and Dynamic power. Activity factor. Power reduction techniques: Clock gating, Power gating, Dynamic voltage scaling.

Transient response of CMOS gates. Delay definitions: rise time, fall time, propagation delay and contamination delay, RC delay model. Effective resistance & capacitance. Elmore delay. Parasitic and effort delay. Fan-in and fan-out. Layout comparisons.

Physical design of ICs: floorplanning, partitioning, routing, clock tree synthesis, KL Algorithm for partitioning, Lee’s algorithm for global routing.

## **Course Resources**

## **Lab software**

* **dsch2**

Download link: [dsch2 (Experiment 1)](https://drive.google.com/file/d/1VxuCTdAymfYEJriKhTRxxYf2mpYKmwAA/view?usp=sharing) (For experiments: 1)

* **Quartus**   
  Download link: [Quartus (Experiment 1, 2, 3)](https://drive.google.com/drive/folders/1VVXijpn4d9LY4PS-Q_dAKXCU8q9xoESm?usp=sharing)(For experiments: 2, 3, 4, 5)
* **Microwind**

Download link: [Microwind (Experiment 6, 7)](https://drive.google.com/drive/folders/11xGLeyzWkfMV4nPgUqLjLi4eXAZVs7WM?usp=sharing)(For experiments: 6)

## **Lab sheets and slides**

<https://drive.google.com/drive/folders/1TNJdG7NT04rOSxk9uAAWgSpq2OQ2hjWE?usp=drive_link>

**Quartus Manual**

<https://docs.google.com/document/d/12wzgwOA7nTLRG_ka7d9aXwsGOYptECSK/edit?usp=drive_link&ouid=105129594214546103693&rtpof=true&sd=true>

## **Textbooks**

[Text Books](https://drive.google.com/drive/folders/1b2knUpNjkgbBkotfHXUuow40OkvpdTrC?usp=drive_link)

* **[Weste&Harris]** CMOS VLSI Design A Circuit and Systems Perspective 4e - Weste, Harris
* **[Brown&Vranesic]** Fundamentals of Digital Logic with Verilog Design 3e - Stephen Brown, Zvonko Vranesic
* **[Andrew,Jens,Igor&Jin]** VLSI Physical Design: From Graph Partitioning to Timing Closure 1e - Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu
* [Naveed A. Sherwani] Algorithms for VLSI Physical Design automation (third edition)

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## **Lecture Slides**

[Theory Lecture Slides](https://drive.google.com/drive/folders/1EPUKHA20XLouHEopMOQbuwkp9QC7U2m-?usp=sharing)

**Lecture Slides (Modified by YAP)**

[Lecture Slides YAP](https://drive.google.com/drive/folders/1mr2goIjWADSGtCODbeXljZBOsvgSfxJe?usp=sharing)

**Lecture Slides (Modified by THL)**

[Lecture Slides THL](https://drive.google.com/drive/folders/1vdJulV6-X9CPb8G-WNBdk7Q-DdQqRymQ?usp=sharing)

**Practice problems sheet**

[CSE460 Practice Problem](https://docs.google.com/document/d/1P4hwfkCCswdx4Tf-BmXoR6tr-HaWm2RD/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

**Topics-Wise Previous Questions**

[CMOS, Digital Electronics, DC response.docx](https://docs.google.com/document/d/10kl5JMteBfSp8msbA9BFcJ2XbGil9t_R/edit?usp=drive_link&ouid=104111303564110437567&rtpof=true&sd=true)

[FSM.docx](https://docs.google.com/document/d/1EVWQiTec9YT8kAkcErsCc-Fa3NnKsiLe/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

[Delay.docx](https://docs.google.com/document/d/1xN3YcZHSGkD0j3mw5S1y6zCSD8sndf9S/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

[KL.docx](https://docs.google.com/document/d/1AeVXWF8FXY_goiKRfVadSngRv7C1jurT/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

[Lee's.docx](https://docs.google.com/document/d/1NaM46sx0MmF2R9xppX5VF90EhaOZkFi6/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

[Delay.docx](https://docs.google.com/document/d/1xN3YcZHSGkD0j3mw5S1y6zCSD8sndf9S/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

[Power.docx](https://docs.google.com/document/d/1yayv05SeH58rTaEaSc8R9MFJnxvzeDmh/edit?usp=sharing&ouid=104111303564110437567&rtpof=true&sd=true)

# **Theory Timeline:**

| No | Topic | Week/Lecture# | **Related CO (if any)** |
| --- | --- | --- | --- |
| 1 | * Introduction to VLSI (Very Large Scale Integration) design: history, IC trends, technology & design approaches. Moore’s law. * Review of digital electronics | Week 1/Lecture 1-2 | CO1 |
| 2 | * Logic circuit families: n-MOS, p-MOS, pseudo n-MOS and CMOS technologies. Introduction to CMOS logic. Pull-up and pull-down networks, implementation using series and parallel MOSFETs. * Implementation of combinational logic blocks and sequential elements in CMOS technology | Week 2/Lecture 3-4 | CO1 |
| 3 | * Pass transistor DC characteristics * Complex gate design using CMOS such as And-Or-Invert or Or-And-Invert. Implementation of different circuit elements like basic gates. Multiplexers, encoder, latch, flip-flops using CMOS Pass transistors.      * Quiz 1 | Week 3/Lecture 5-6 | CO1 |
| 4 | * FSM Introduction * FSM moore and mealy type machine | Week 4/Lecture 7-8 | CO2 |
| 5 | * System design using moore and mealy type finite state machines * Different hardware implementation techniques * Quiz 2 | Week 5/Lecture 9-10 | CO2 |
| 6 | Reserved for Quiz 1+2 | Week 6 | CO1, CO2 |
| 7 | Midterm Exam | Week 7 | CO1, CO2 |
| 8 | * Physical design: floor planning, partitioning, routing, clock tree synthesis. KL algorithm for partitioning. | Week 8/Lecture 11-12 | CO4 |
| 9 | * Lee’s maze algorithm for global routing | Week 9/Lecture 13-14 | CO4 |
| 10 | * Transient response of CMOS gates. Delay definitions: rise time, fall time, propagation delay and contamination delay, RC delay model. Effective resistance. MOS Capacitance. * Quiz 3 | Week 10-/Lecture 15-16 | CO3 |
| 11 | * Elmore delay. Parasitic and effort delay. Fan-in and fan-out. Layout comparisons | Week 11/Lecture 17-18 | CO3 |
| 12 | * CMOS Power: Instantaneous and Average power, Energy. Power in circuit elements analysis (R, C, DC Supply). Switching waveforms of an inverter. Static power and Dynamic power. Activity factor. Power reduction techniques: Clock gating, Power gating, Dynamic voltage scaling. * Quiz 4 | Week 12/Lecture 19-20 | CO3 |
| 13 | Reserved for Quiz 3+4 | Week 13 | CO3, CO4 |
| 14 | Final Exam | Week 14 | CO3, CO4 |

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# **Lab Timeline**

| **No** | **Topic** | **Week/Lecture#** | **Related CO (if any)** |
| --- | --- | --- | --- |
| 1 | No lab | Week 1 | - |
| 2 | Experiment 1: CMOS Schematic Circuit Design in DSCH2 | Week 2 | CO1 |
| 3 | Experiment 2: Introduction to Verilog; Verilog Design Part 1 (combinational logic) | Week 3 | CO1 |
| 4 | Experiment 3: Verilog Design Part 2 (sequential logic) | Week 4 | CO1 |
| 5 | Reserved | Week 5 | - |
| 6 | Midterm | Week 6 | - |
| 7 | Lab Test-1 | Week 7 | CO1 |
| 8 | Experiment 4: Verilog Design Part 3 (FSMs) | Week 8 | CO2 |
| 9 | Experiment 5: Verilog Design Part 4 (FSMs) | Week 9 | CO2 |
| 10 | Assessment on Experiment 5 | Week 10 | CO2 |
| 11 | Lab Test-2 | Week 11 | CO2 |
| 12 | Reserved | Week 12 | - |
| 13 | Reserved | Week 13 | - |
| 14 | Final | Week 14 | - |

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**BuX Video Link**

| **BuX Video Link** |
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| 1. [Course Content](https://www.youtube.com/watch?v=mJu9fpg3MbI)  2. [The transistor concept](https://www.youtube.com/watch?v=UAyXRaHNL1k)  3.[History and basic transistor](https://www.youtube.com/watch?v=BKh7z2kx6ec)  4.[MOSFETs: A closer look](https://www.youtube.com/watch?v=xgQmFFLcIsw)  5.[Moore's Law](https://www.youtube.com/watch?v=qeDwCbBLGY0)  6.[Design abstraction and methodologies](https://www.youtube.com/watch?v=5oXYlS-uYEI) |
| 1.[Review of logic gates](https://www.youtube.com/watch?v=RcxuKJAIqg8)  2.[Logic function synthesis (SOP, POS, K-maps)](https://www.youtube.com/watch?v=hcCqpXwRtpA)  3.[Review of MUX](https://www.youtube.com/watch?v=g_piW_cVMg8)  4.[Review of Mux, Decoder and Encoder (optional)](https://www.youtube.com/watch?v=laWRIyPDOeI)  5.[Review of D latch](https://www.youtube.com/watch?v=GPSxuZvVPU4)  6.[Review of D flip-flop](https://www.youtube.com/watch?v=Dh_KKtuWgjI)  7.[Level triggered vs. Edge triggered](https://www.youtube.com/watch?v=dFNgRTbCTGU) |
| 1.[CSE 460 Experiment 4 Part 1 : Introduction to DSCH2](https://www.youtube.com/watch?v=pqQqr5TT7to)  2.[CSE 460 Experiment 4 Part 2 : DSCH2 Example - CMOS Inverter](https://www.youtube.com/watch?v=Zo1nCareFJ8)  3.[CSE 460 Experiment 4 Part 3 : DSCH2 Example - F= AB+CD](https://www.youtube.com/watch?v=ZoMN5kF-sgQ)  4.[CSE 460 Experiment 4 Part 4 : DSCH2 Example - NAND gate](https://www.youtube.com/watch?v=wPnnReoL0D4)  5.[DSCH2 Example - D latch](https://www.youtube.com/watch?v=-HablBLtRcQ)  6.[DSCH2 Example D Flip Flop](https://www.youtube.com/watch?v=bHnZYKDDkr8) |
| 1. [460 L3 P1](https://www.youtube.com/watch?v=DcNluKKrmdI)  2. [nMOS and pMOS operation](https://www.youtube.com/watch?v=I84v0g4M4iU)  3. [CMOS logic gate general structure: part 1](https://www.youtube.com/watch?v=RICvIDHU0yk)  4.[CMOS logic gate general structure: part 2](https://www.youtube.com/watch?v=03UXvgaKYsk)  5.[Example 1](https://www.youtube.com/watch?v=YurhPT9l0Vo)  6.[Example 2](https://www.youtube.com/watch?v=xju8NFb-jT4)  7.[Example 3](https://www.youtube.com/watch?v=8bM7ltfNUjw) |
| 1.[nMOS and pMOS as pass transistors](https://www.youtube.com/watch?v=l588g6kTwig)  2.[CMOS Transmission gates](https://www.youtube.com/watch?v=eR0RgGKGWTI)  3.[CMOS Tristate buffers and inverters](https://www.youtube.com/watch?v=1zSZ75jp3MQ)  4.[CMOS Multiplexers](https://www.youtube.com/watch?v=5NE5ESZMDuo)  5.[CMOS D Latch](https://www.youtube.com/watch?v=S-do28E3BlQ)  6.[CMOS D Flip-flop](https://www.youtube.com/watch?v=LzSno4vso0c) |
| 1.[MOS Operating modes](https://www.youtube.com/watch?v=PHV7yF5AM1k)  2.[nMOS Regions of operation](https://www.youtube.com/watch?v=fu4VgF6Yj38)  3.[nMOS I-V Characteristics derivation: part 1](https://www.youtube.com/watch?v=mgUwWoxa670)  4.[nMOS I-V Characteristics derivation: part 2](https://www.youtube.com/watch?v=VEDUqNQQLw4)  5.[MOSFET I-V Characteristics Summary](https://www.youtube.com/watch?v=0DYm0zd_JRk) |
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| 1.[nMOS & pMOS I-V Characteristics Summary](https://www.youtube.com/watch?v=bnFmbeTG_Z8)  2.[Example 1](https://www.youtube.com/watch?v=JFfd-s8V0Kc)  3.[Example 2](https://www.youtube.com/watch?v=Rplae-SphQ4)  4.[Example 3](https://www.youtube.com/watch?v=foE8v2WImDs)  5.[Gate and diffusion capacitance](https://www.youtube.com/watch?v=opvHrOObotE) |
| 1.[DC Response](https://www.youtube.com/watch?v=bPZWBu3dURU)  2.[CMOS Inverter DC Response Derivation](https://www.youtube.com/watch?v=a7DTGNqh5Hw)  3.[DC Response Practical Considerations](https://www.youtube.com/watch?v=Y2RGHQWCDLY) |
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